IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

Objections to Drawings

The drawings have been objected to for failing to show the subject matter of claim 9. This objection is respectfully traversed. FIG. 1 in conjunction with FIG. 2 of Applicant's Specification provides support for the limitations of claim 9:

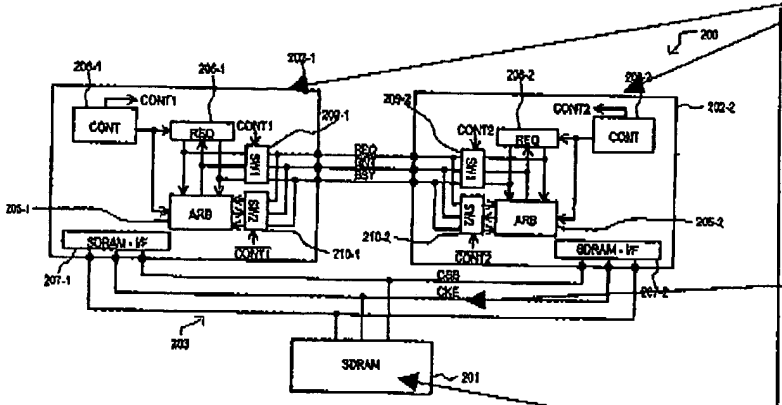

FIG. 1

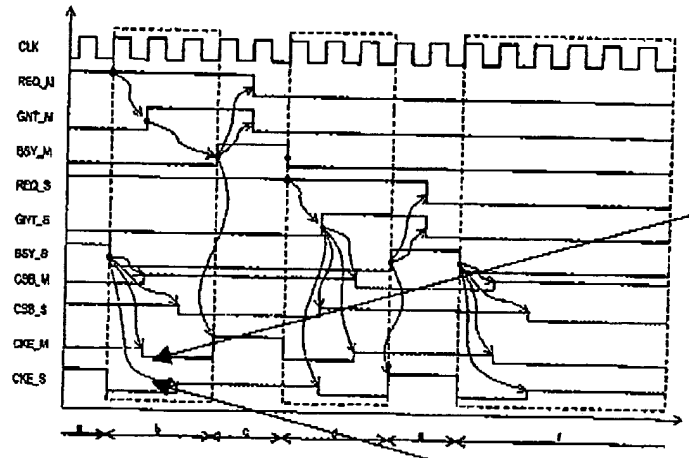

FIG. 2

A plurality of data processing circuits (202-1 and 202-2) that share access to the semiconductor memory circuit, each having a

At least one control line (CKE) coupled to the control input of the semiconductor memory

A semiconductor memory (201) that is controlled by inputs to at least one control input

When one data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal (CKE_M) at its control output at the predetermined potential within the first time period.

When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal (CKE_S) at the control output at a predetermined potential for a first time period before ending the control signal

Control signals CKE_M (provided from master data processing circuit **202-2**) and CKE_S (provided from slave data processing circuit **202-1**) have an operation described in the Specification on page 13, lines 3-21 set forth below with emphasis added. It should be noted that the subscript "_S" indicates a signal originating from a slave and the subscript "_M" indicates a signal originating from a master as clearly indicated on page 12, lines 15-17 of the Specification. However, it is understood that these signals share the same control line (control line CKE in FIG. 1).

> In a time period "b", processing for a slave data processing circuit **202**-2 can end, and processing can migrate from a slave data processing circuit **202**-2 to a master data processing circuit **202**-1. ***When processing for the slave data processing circuit 202-2 ends***, a controller **208**-2 can supply requester **206**-2 and I/F circuit **207**-2 with an end signal END. A requester **206**-2, after receiving an END signal, can set busy signal BSY_S to inactive (low, in this example). I/F circuit **207**-2, after receiving an END signal, ***can set a clock enable signal CKE_S to inactive (low, in this example)***.
>
> An arbiter **205**-1 on a master side can respond to the inactive state of the busy signal BSY_S to supply a grant signal GNT_M. Grant signal GNT_M can be based on a request signal REQ_M on a master side. It is understood that request signal REQ_M from a master side will have priority over a request signal REQ_S from a slave side.
>
> Referring still to time period "b" of FIG. 2, ***one clock cycle following the transition of busy signal BSY_S to an inactive state***, I/F circuit **207**-1 on a master side can set a chip select signal CSB_M from the master side to a high level, and ***can set a clock enable signal CKE_M to low level.***
>
> Then, ***two clock cycles following the transition of busy signal BSY_S*** to an inactive state, I/F circuit **207**-2 on a slave side ***can set*** a chip select signal CSB_S and ***clock enable signal CKE_S to a high impedance (hi-Z) state (i.e., outputs on a slave side that provide such signals can be set to a hi-Z state)***.

The above description in conjunction with FIGS. 1 and 2, clearly show that when processing for the slave data processing circuit (i.e. one data processing circuit) ends, a clock enable signal CKE_S is set to a low level (i.e. a predetermined potential) for two clock cycles (a

predetermined time period). One clock cycle into the predetermined time period (note this is subsequent to processing for the slave data processing circuit ending), the master data processing circuit sets a clock enable signal CKE_M to a low level. Then, at the end of the predetermined time period, slave data processing circuit sets clock enable signal CKE_S to a high impedance state. In this way, control of the memory device is transferred from the slave data processing circuit to the master data processing circuit.

Applicant strongly stresses that the above represents but one example of how the limitations of claim are illustrated in a specific embodiment. That is, the illustrated embodiment should not be construed as limiting to the claims, as the subject matter of claim 9 could take various other forms.

Objections to Claims 9 and 15.

To address this objection, the above explanation with respect to the objections to the drawings are incorporated by reference to illustrate adequate support in the Specification for claim 9.

The objection to claim 15 will now be addressed.

Claim 15 is directed to a method of sharing a semiconductor memory circuit with a plurality of data processing circuits including the steps of:

(1) when a data processing circuit ends control of the semiconductor memory circuit, driving control outputs coupled to control lines for the semiconductor memory circuit to predetermined logic values, and subsequently placing the control outputs in a high impedance state.

(2) When a data processing circuit starts control of the semiconductor memory circuit, driving control outputs coupled to control lines to the predetermined logic values prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit being placed in the high impedance state.

Step (1) above is illustrated below with reference to FIG. 2, in conjunction with page 13, lines 3-9 and 18-21 of the Specification shown below (*emphasis added*).

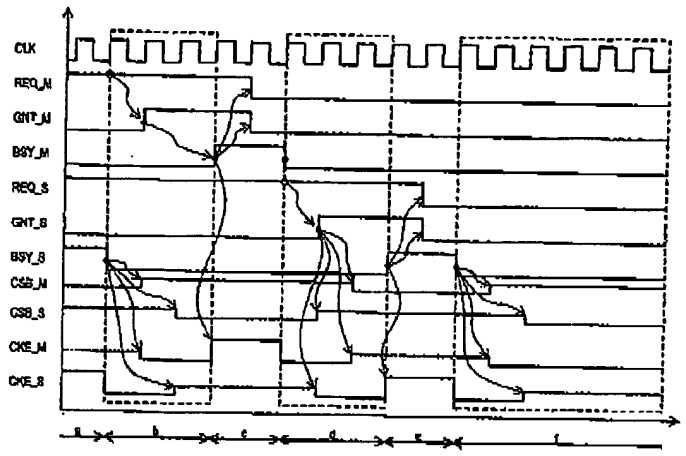

FIG. 2

In a time period "b", processing for a slave data processing circuit 202-2 can end, and processing can migrate from a slave data processing circuit **202**-2 to a master data processing circuit **202**-1. When processing for the slave data processing circuit **202**-2 ends, a controller **208**-2 can supply requester **206**-2 and I/F circuit **207**-2 with an end signal END. A requester **206**-2, after receiving an END signal, can set busy signal BSY_S to inactive (low, in this example). I/F circuit **207**-2, ***after receiving an END signal, can set a clock enable signal CKE_S to inactive (low, in this example).***

Then, ***two clock cycles following the transition of busy signal BSY_S*** to an inactive state, I/F circuit **207**-2 on ***a slave side can set a chip select signal CSB_S and clock enable signal CKE_S to a high impedance*** (hi-Z) state (i.e., outputs on a slave side that provide such signals can be set to a hi-Z state).

Step (2) above is illustrated with reference to FIG. 2 in conjunction with page 13, lines 14-17 of the Specification below (*emphasis added*).

Referring still to time period "b" of FIG. 2, ***one clock cycle following the transition of busy signal*** BSY_S to an inactive state, I/F circuit **207**-1 on ***a master side can set a chip select signal CSB_M from the master side to a high level, and can set a clock enable signal CKE_M to low level.***

In this way, when a data processing circuit (202-2) ends control of the semiconductor memory circuit (201), control outputs (CKE_S and CSB_S) can be driven to predetermined logic values and subsequently placed in a high impedance state (hi-Z state). When a data processing circuit (202-1) starts control of the semiconductor memory circuit, control outputs (CKE_M and CSB_M) are driven to the predetermined logic values prior to the control outputs (CKE_S and CSB_S) of the data processing circuit (202-2) that is ending control of the semiconductor memory circuit (201) being placed in the high impedance state.

Accordingly, Applicant believes that invention of claims 9 and 15 are clearly supported by the specification and the objections should be withdrawn.

Again, Applicant strongly stresses that the above represents but one example of how the limitations of claim are illustrated in a specific embodiment.

Rejection of Claims 1, 3, 5, 9, 10, and 14-17 Under 35 U.S.C. §103(a), based on Applicant's Background Art (BACKGROUND ART) in view of *Wilcox et al.* (USP 6,510,099).

The rejection of claims 1, 3, and 5 will first be addressed.

Claim 1 has been amended to clarify an element of the invention.

The invention of amended claim 1 is directed to a data processing apparatus that arbitrates sharing of a single semiconductor memory circuit among multiple data processing circuits. The data processing apparatus includes a semiconductor memory circuit and a data processing circuit supplies the semiconductor memory circuit with a clock enable signal and a chip select signal. In the data processing apparatus, before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with the clock enable signal and chip enable signal having clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

[1] MPEP §2143.

The rejection admits that the BACKGROUND ART does not disclose "before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the clock enable signal and chip select signal, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory with the clock enable signal and chip enable signal having clock enable signal and chip select signal values at the same state as those provided by the data processing circuit ending control of the semiconductor memory circuit", as recited in claim 1.[2]

However, the other reference relied upon by the rejection, *Wilcox et al.*, does not show such a limitation, either.

Wilcox et al. shows a single memory controller (106) providing control lines (324) to a plurality of memory devices in a memory system (110).[3] *Wilcox et al.* also shows that the control lines (324) include first and second chip select signal (CS_1 and CS_2) and first and second clock enable signals (CKE_1 and CKE_2). Signals CS_1 and CKE_1 go to one row of DDR SDRAM memory devices and CKE_2 go to a second row of DDR SDRAM devices.

Thus, *Wilcox* shows only one controller sharing a number of memory devices and providing signals to a memory bus (114). That is, there is no other device (i.e., controller, data processing circuit) that "starts control" of any memory device from the memory controller (106). All other devices (i.e. processor 102, graphic controller 120, and I/O controller 108) are connected to the memory controller (106) and not to the memory system (110), therefore, the memory controller must always maintain control over the memory system (110).

This is illustrated in the below figure of the reference:

[2] See page 5, first paragraph of Office Action dated 9/21/2005.
[3] See FIG. 3 of *Wilcox et al.* showing a memory controller (106) providing control lines (324) to memory system (110).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

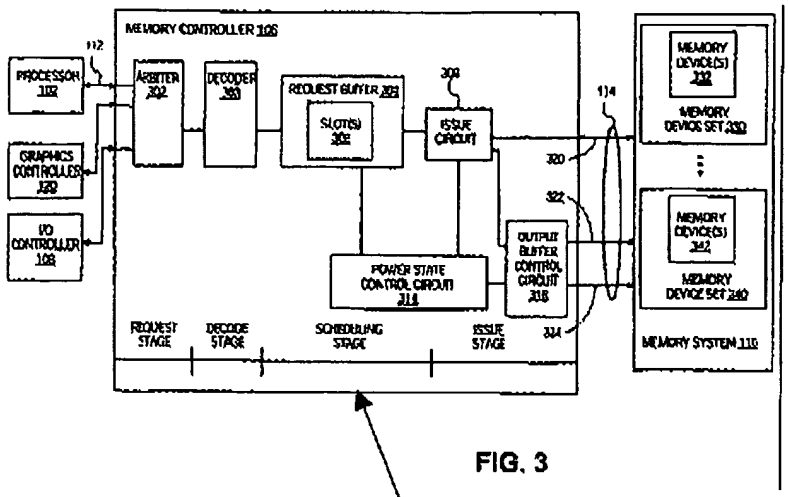

FIG. 3

See FIG. 3 of *Wilcox et al.* above, memory controller 106 is the only element connected to memory system (110) and therefore must always maintain control over memory system (110). Nowhere is it shown "a different data processing circuit starting control of a semiconductor memory circuit and supplying the semiconductor memory circuit with the clock enable and chip enable signal ... before the data processing circuit ends control of the semiconductor memory".

For these reasons, *Wilcox et al.* is not believed to show "a different data processing circuit starting control of a semiconductor memory circuit and supplying the semiconductor memory circuit with the clock enable signal and chip enable signal" "before the data processing circuit ends control of the semiconductor memory" according to the claimed signal activations, as recited in amended claim 1.

Further, because both reference appear silent as to such control switching operations of a clock enable signal and chip select signal from one data processing circuit to another data processing circuit, the cited combination of references is not believed to be suggestive of such a limitation, either.

For all of these reasons, the combination of references is not believed to show or suggest all the limitations of amended claim 1, and this ground for rejection are traversed.

The rejection of claims 9, 10, and 14 will now be addressed.

The data processing apparatus of amended claim 9 includes a semiconductor memory circuit that is controlled by control signal inputs to at least one control input. At least one control

line is coupled to the at least one control input of the semiconductor memory circuit. A plurality of data processing circuits that share access to the semiconductor memory circuit, each data processing circuit having a control output coupled to the at least one control line. When one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal. Subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "another data processing circuit" taking control over a semiconductor memory circuit from a first data processing circuit according to the control signal potentials and time periods, as recited in claim 9. In particular, *Wilcox et al.* shows a memory controller (106) always maintaining control over a memory system (110).

Claim14, which depends from claim 9, is believed to be separately patentable over the cited reference. Claim 14 recites that "at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits".

The rejection relies on the BACKGROUND ART to show the limitations of claim 14. Applicant does not believe such teachings are shown or suggested. Applicant's FIG. 4 of the BACKGROUND ART shows two controllers 102 (i.e., data processing circuits) that provide signals via signal lines (106) and data buses (105). However, no signal lines (106) of one controller are directly connected to the outputs of multiple data processing circuits. Instead, such signals lines (106) are commonly provided to arbiter (103). Similarly, no bus lines (105) of one controller are directly connected to the outputs of multiple controllers. Instead, data buses (105) are commonly provided to bus control circuit (104).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

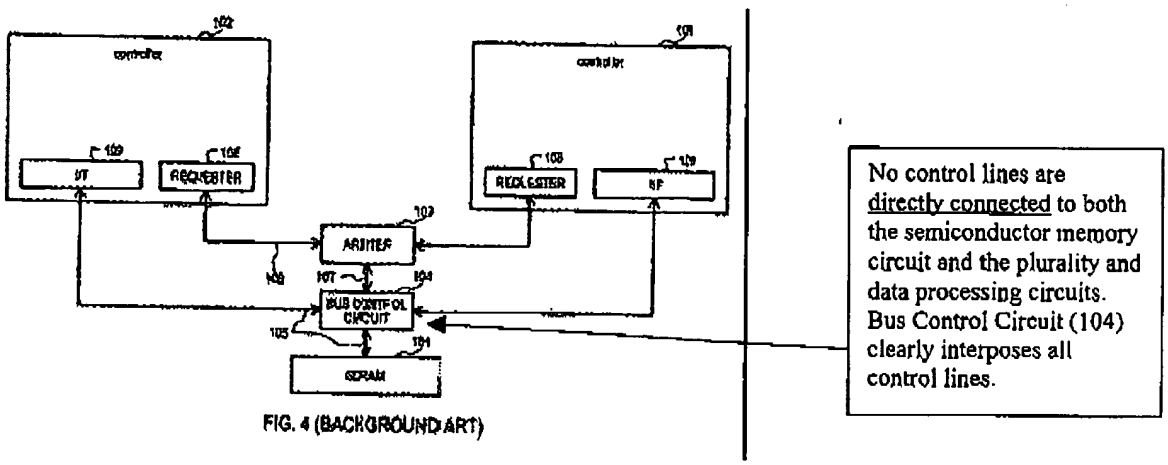

FIG. 4 (BACKGROUND ART)

Because the BACKGROUND ART only teaches connection to an interposing circuit, the reference is not believed to shows or suggests a direct connection, as recited in claim 14, either.

For these reasons, the combination of references is not believed to show or suggest all the limitations of claim 14, and this ground for rejection is traversed.

The rejection of claims 15–17 will now be addressed.

The invention of amended claim 15 is directed to a method of sharing a semiconductor memory circuit with a plurality of data processing circuits. The method includes, when a data processing circuit ends control of the semiconductor memory circuit, driving control outputs connected to control lines for the semiconductor memory circuit to predetermined logic values, and subsequently placing the control outputs in a high impedance state. The method also includes, when a data processing circuit starts control of the semiconductor memory circuit, driving control outputs connected to the control lines to the predetermined logic values prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit being placed in the high impedance state.

To address this rejection, the arguments set forth with regard to claim 1 are incorporated herein by reference. Namely, neither reference shows or suggests "when a different one of the plurality of data processing circuits starts control of the semiconductor memory circuit, driving control outputs prior to the control outputs of the data processing circuit that is ending control of the semiconductor memory circuit". Rather, the teachings relied upon to show the limitations of claim teach only a single controller controlling multiple memory devices.

To further address this rejection, the arguments set forth with regard to claim 14 are incorporated herein by reference. Namely, neither reference shows or suggests the control lines connected to both the data processing circuit that ends control of the semiconductor memory circuit and the data processing circuit that starts control of the semiconductor memory circuit. Both references show intervening circuits between the control lines.

Accordingly, because the cited combination of references is not believed to show or suggest all of the Applicant's claim limitations, this ground for rejection is traversed.

Rejection of Claims 4, 7, 11 and 18-20 Under 35 U.S.C. §103, based on Applicant's Background Art in view of *Wilcox et al.*, and further in view of *Askinazi et al.* (USP 4,453,21).

The rejection of claims 4 and 7 will first be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the same general comments set forth above for independent claim 1.

The rejection of claim 11 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the same general comments set forth above for independent claim 9.

The rejection of claim 18-20 will now be addressed.

To the extent that this ground for rejection relies on the combination of the BACKGROUND ART in view of *Wilcox et al.*, Applicant incorporates by reference herein the comments set forth above for independent claim 15.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Claims 1 has been amended not in response to the cited art, but to clarify an element of the invention. No new matter has been added. Claim 15 has been amended to include limitations found in claim 14, therefore a new search is not required.

The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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